Low-Complexity Adaptive MIMO Equalizer With Hybrid-Precision Tap Bit-Width Optimization for Hardware-Efficient 200G Coherent PON

Wenqing Jiang, Chenyang Han, Yongxin Xu, Xiaokai Guan, Xudong Wang, Weisheng Hu, and Lilin Yi

***Abstract*—The adaptive multiple-input multiple-output (MIMO) equalizer deployed in coherent receivers can compensate for channel impairments in passive optical networks (PONs). The polarization rotation, chromatic dispersion, and device bandwidth limitation are effectively mitigated. However, the implementation of electronic adaptive MIMO equalizers in application-specific integrated circuits (ASICs) becomes increasingly challenging due to the substantial complexity with higher signal rates. To overcome this problem, we propose a hybrid-precision fixed-point quantization strategy that reduces the total tap bit-width, thereby lowering the hardware computational complexity. The genetic algorithm (GA) is employed to determine the optimal bit-width configuration. Moreover, for taps with minor magnitudes, redundant high-order bits are removed through left-shift operations to reduce the bit-width further. The simplified architecture is adapted to field-programmable gate array (FPGA) deployment. In the FPGA implementation, employing shared feedback modules for multi-channel tap coefficient updates can eliminate the structural redundancy. Finally, the proposed scheme is experimentally demonstrated in a C-band band-limited 200-Gbps coherent PON system. A 57.20% average reduction in resource utilization, accompanied by 0.60-dB and 0.62-dB power budget penalties in X and Y polarizations, is achieved when the signal-to-noise ratio (SNR) loss threshold for bit-width optimization is 0.4 dB after removing redundant bits. The optimized equalizer is employed in the 50-channel deployment to achieve a real-time rate of 100 Gb/s. The power budgets in X and Y polarizations, at 33.73 dB and 33.63 dB, respectively, are attainable with a power consumption of 38.2 W.**

***Index Terms*—Field-programmable gate array, fixed-point quantization, genetic algorithm, passive optical network.**

I. Introduction

RECENTLY, the exponential growth of global data traffic has been predominantly driven by 5G deployments, the proliferation of the Internet of Things (IoT), cloud computing services, and large-scale artificial intelligence (AI) models. Meanwhile, the rate of passive optical networks (PONs) has been growing significantly [1], [2], [3], [4], [5], [6]. The 50G PON standards have been finalized, enabling large-scale commercial deployment. The ITU-T is currently developing standards for next-generation 200G PON. Compared to the intensity modulation and direct detection (IMDD) technique, coherent detection has no rate risk since it leverages both phase and polarization, thereby becoming one of the most powerful solutions for 200G PON [7], [8], [9]. However, channel impairments in coherent systems, including polarization rotation, chromatic dispersion (CD), frequency offset (FO), and phase noise, require a more complex digital signal processing (DSP) algorithm for compensation to improve the signal quality. This significantly increases ASIC chip power consumption and area, resulting in higher operating temperature and integration challenges. Therefore, it is necessary to reduce the complexity of adaptive multiple-input multiple-output (MIMO) equalizers, which are one of the most power-consuming components.

There have already been related works proposing a simplified structure of adaptive MIMO equalizers. By cascading a 1-tap butterfly equalizer with polarization-independent filters, the reduction in finite impulse response (FIR) filter count is achieved [10], [11], [12], [13]. The architecture is implemented on a field programmable gate array (FPGA), achieving 10-Gb/s real-time equalization in [14]. To address degraded differential group delay (DGD) compensation in 1-tap butterfly equalizers, a cascaded few-tap butterfly equalizer and long polarization-independent FIR filters structure is proposed [15], [16]. Furthermore, the fixed-coefficient FIR filters are used to eliminate the update module, enabling 5-Gb/s real-time dual-polarization quadrature phase-shift keying (DP-QPSK) equalization on a graphics processing unit (GPU). The real-valued equalizers are adopted to avoid high-complexity complex multiplications [17], [18], [19]. The FPGA-based 5 Gb/s real-time equalization is implemented, and the number of multipliers is reduced by 47% [19]. In [20], [21], multipliers are decomposed into sign decision, shift operations, and accumulation to achieve the real-time 10 Gb/s DP-QPSK transmission. In the feedback, the block constant modulus algorithm (CMA) is used to reduce the tap update frequency [22]. Additionally, the error term based on power-of-two quantization

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The authors are with the State Key Laboratory of Photonics and Communications, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: sjtujwq@sjtu.edu.cn; hanchenyang@sjtu.edu.cn; xuyongxin@sjtu.edu.cn; guanxiaokai@sjtu.edu.cn; xudongwang.7hqq@sjtu.edu.cn; wshu@sjtu.edu.cn; lilinyi@sjtu.edu.cn).

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is adopted to diminish the update computation complexity [23]. For machine learning, the bidirectional long-short-term memory (bi-LSTM) coupled with a convolutional neural network (CNN) equalizer is implemented in an FPGA for the first time [24]. The Taylor series, piecewise linear, and look-up table (LUT) approximations are employed to approximate the activation function of NN. These methods simplify the adaptive MIMO equalizer structurally or computationally. However, the bit-width optimization is orthogonal to such structural simplifications and should be employed to realize chip-adapted algorithms, which is an essential approach for reducing the hardware cost.

Therefore, we propose a hardware-efficient adaptive MIMO equalizer based on hybrid-precision tap bit-width optimization. The genetic algorithm (GA) is employed to determine the optimal bit-width allocation. The bit-width of taps with minor impact on performance is clipped to reduce the complexity. The essential taps retain a higher bit-width to ensure the precision. The simplified architecture is adapted to the hardware implementation. Additionally, the high-order bits containing no information in minimally valued taps are eliminated through left-shift operations to further compress the bit-width. The efficiency of the proposed scheme is verified in a 1550-nm coherent PON system transmitting the 200-Gbps dual-polarization 16-quadrature amplitude modulation (DP-16QAM) signal. The simplified 21-tap MIMO equalizer is deployed in an FPGA with programmability and a short iteration cycle for rapid design and verification of ASIC chip prototypes. In addition, the parallelization of an FPGA can provide high-speed signal processing ability. In parallel implementation, the shared error calculation and coefficient update modules are adopted to reduce the feedback complexity. The results show that compared with the reference model featuring 16-bit taps, the average resource consumption is reduced by 57.20% with a 0.4-dB signal-to-noise ratio (SNR) loss threshold after removing redundant bits. Finally, we implement the simplified 21-tap MIMO equalizer with 50 parallel channels corresponding to a 100-Gbps real-time rate in an FPGA. The power consumption is 38.2W, achieving power budgets in X and Y polarizations of 33.73 dB and 33.63 dB.

The rest of this paper is organized as follows. Firstly, the principles of adaptive MIMO equalizer and fixed-point quantization are introduced in Section II. Then, the bit-width optimization of taps is presented in Section III. Next, the multi-channel implementation of the MIMO equalizer is introduced in Section IV. The experimental setup and results are illustrated in Section V. Finally, we conclude this work in Section VI.

II. Principles of MIMO Equalizer and Fixed-Point Quantization

The block diagram of a dual-polarization adaptive MIMO equalizer is shown in Fig. 1. The structure comprises feedforward and feedback modules. The feedforward module consists of four parallel FIR filters, denoted as hxx, hxy, hyx, and hyy. The polarization rotation, chromatic dispersion (CD), and device bandwidth limitation in the fiber channel are compensated to enhance the performance of high-speed optical coherent

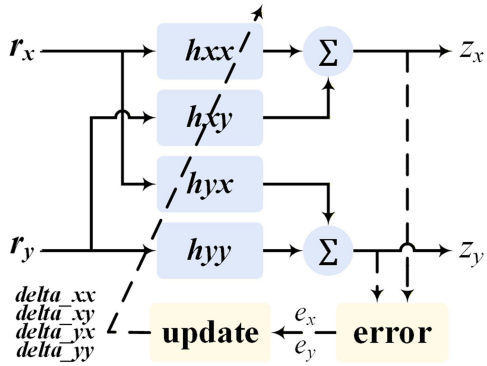

Fig. 1. The block diagram of a dual-polarization adaptive MIMO equalizer.

communication systems. The feedback module includes error computation and coefficient update sections, enabling the real-time tracking of channel variations.

The received signals for X- and Y-polarizations are denoted as r_x and r_y, respectively. Then, the output signals are defined as

$$\begin{cases} z_x(k) = \sum_{n=-N}^{N} h_{xx}(n) \cdot r_x(k-n) + h_{xy}(n) \cdot r_y(k-n) \\ z_y(k) = \sum_{n=-N}^{N} h_{yx}(n) \cdot r_x(k-n) + h_{yy}(n) \cdot r_y(k-n) \end{cases} \tag{1}$$

where $2N+1$ is the memory length of the adaptive MIMO equalizer. The linear impairments are compensated by the hxx and hyy filters. The polarization crosstalk is mitigated through hxy and hyxfilters.

The radius directed equalization (RDE) is employed for error calculation [25]. The error metric is based on the Euclidean distance between the equalizer output and the nearest constellation circle radius. The error signal e_p is defined as

$$e_p = z_p(k) \cdot \left(|R_k|^2 - |z_p(k)|^2 \right) \ (p = x \text{ or } y) \tag{2}$$

The R_k represents the radius of the constellation circle closest to $z_p(k)$. The tap weight vector is adaptively updated based on the stochastic gradient descent (SGD) algorithm, which is expressed as

$$\boldsymbol{h_{pq}} = \boldsymbol{h_{pq}} + \mu \cdot e_p \cdot conj(\boldsymbol{r_q}) \ (p, q = x \text{ or } y) \tag{3}$$

where $\boldsymbol{h_{pq}} = [h_{pq}(-N), h_{pq}(-N+1), \ldots, h_{pq}(N)]^T$ is the tap weight vector of the equalizer, and the $\boldsymbol{r_q} = [r_q(-N), r_q(-N+1), \ldots, r_q(N)]^T$ is the input signal vector of X- or Y- polarization. The μ is the step size, and $\mathrm{conj}(\cdot)$ represents the complex conjugate operation.

The equalizer is typically implemented in ASICs. Therefore, the floating-point numbers should be converted to fixed-point numbers for hardware deployment [26]. The signed numbers are represented in two's complement format, consisting of sign, integer, and fractional bits. The $Qm.n$ format is adopted for representing the fixed-point quantization of floating-point numbers, where $m$and n denote the integer and fractional bit-widths, respectively. The total bit-width b is calculated as $b = m + n + 1$. This format enables the precise numerical

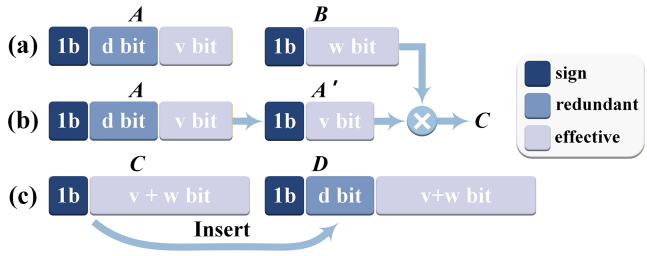

Fig. 2. The scheme for removing the redundant bits by the left-shift operation.

equivalence between the original floating-point number f and the corresponding fixed-point number. The $Qm.n$ format of f is numerically equivalent to

$$f_{Qm.n} = round\,(f \cdot 2^n) \cdot 2^{-n} \tag{4}$$

where $round(\cdot)$is the rounding operation. Then, the $f_{Qm.n}$ is converted to the fixed-point number as

$$f_{bin} = dec2bin\,(f_{Qm.n}) \tag{5}$$

where $dec2bin(\cdot)$denotes the decimal-to-binary conversion. For example, the floating-point number 1.76 can be represented in Q3.4 fixed-point format as

$$1.76_{bin} = dec2bin\ (1.76_{Q3.4}) = 0001.1100 \tag{6}$$

The quantization error in fixed-point quantization originates from the approximation of floating-point numbers by the finite bit-width, and the magnitude depends on the fractional bit-width n. The error e can be computed as

$$e = f - f_{Qm.n} \tag{7}$$

Generally, the larger n results in the smaller error and higher precision. However, when the fractional bit-width n continues to increase, the precision improvement becomes negligible. Meanwhile, the larger bit-width requires more storage space, and the additional computational resources are consumed during arithmetic operations in the hardware implementation. Therefore, the fractional bit-width n should be minimized while maintaining the required precision to reduce the hardware resource usage and lower the power consumption in the ASIC chip.

Moreover, the fixed-point representation of the decimal number a within the range $(-2^{-d},\ 2^d)$ contains d redundant bits, where d represents a positive integer. The redundant bits exhibit the same value as the sign bit, which can be removed through a d-bit left-shift operation according to

$$a' = a \cdot 2^d \tag{8}$$

where a' is the shifted number, consuming less storage and computational resources.

As shown in Fig. 2(a), the left region represents the sign bit. The central and right regions indicate the redundant and effective bits, respectively. The fixed-point number A consists of one sign bit, d redundant bits, and v effective bits. The fixed-point number Bcontains one sign bit and w effective bits. The redundant bits of A can be removed according to (8), resulting in A', as illustrated in Fig. 2(b). The C is obtained by multiplying A' and B, containing two sign bits and $v + w$ effective bits. To correct the bit-width, a d-bit sign extension is applied to C to obtain the correct fixed-point product result D, as shown in Fig. 2(c). The elimination of redundant bits decreases the computational complexity, thereby reducing the hardware resource consumption.

III. Bit-Width Optimization for Hardware-Efficient Adaptive MIMO Equalizers

For (1), the method described in Section II can be applied to reduce the tap bit-widths of hxx, hxy, hyx, and hyy, thereby decreasing the resource consumption. However, the contributions of different taps to the result vary significantly. Uniformly reducing the fractional bit-widths of all taps leads to substantial precision loss. Therefore, the rational bit-width allocation is required. The larger bit-widths should be allocated to the taps with greater impact on the result, while insignificant taps are assigned fewer bits. This approach reduces the total bit-width while maintaining the accuracy, thus lowering the computational complexity. Moreover, the taps farther from the center exhibit smaller magnitudes, leading to more redundant bits after the fixed-point quantization. The redundant bits can be eliminated using the method as shown in Fig. 2, further reducing the hardware resource consumption.

Fig. 3(a) illustrates the bit-width distribution of the equalizer taps. The left region indicates the sign bit. The central and right regions represent redundant and effective bits, respectively. Typically, the central taps contributing more significantly to the result exhibit larger coefficient magnitudes. In contrast, the marginal taps have smaller coefficients with minor impact on the output. Thus, more fractional bit-widths are allocated to central taps to maintain the performance, while the marginal taps are assigned fewer bits to reduce the hardware overhead, as shown in Fig. 3(b). In addition, the redundant bits are clipped by (8) as shown in Fig. 3(c). The final bit-width configuration is adopted for subsequent hardware deployment of the equalizer. It should be emphasized that the bit-width optimization process is exclusively applied to the fractional part, while the integer part remains unchanged.

A. Optimal Bit-Width Configuration Search Based on Genetic Algorithm

The bit-width optimization is formulated as a discrete, high-dimensional combinatorial optimization problem, and the relationship between the bit-width configuration and system performance lacks an analytic gradient. Due to the absence of an analytic gradient and the computational intractability of exhaustive search, a gradient-free global optimization method is thus required. The genetic algorithm (GA) is particularly appropriate for this problem. Inspired by biological evolution [27], the GA efficiently navigates the complex solution space through its population-based parallel search mechanism. System constraints are naturally incorporated into its fitness function. The total bit-width for taps is minimized without compromising the precision by the GA. In the optimization process, the

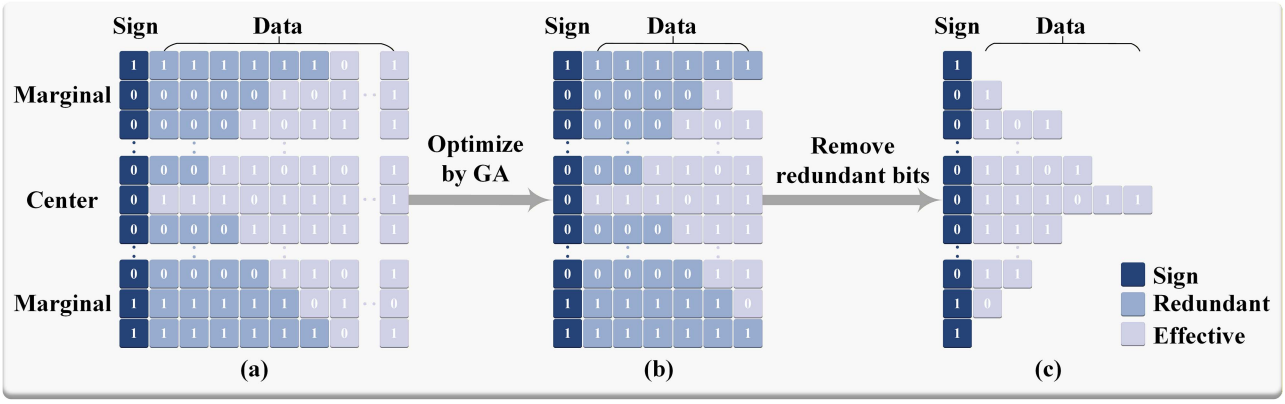

Fig. 3. The process of the bit-width optimization and redundant bit removal.

fractional bit-width vector is encoded as

$$\boldsymbol{bw} = [bw_1, bw_2, \ldots, bw_N] \ (\forall i, \ bw_i \in Z, \ 0 \le bw_i \le ub) \tag{9}$$

where bw_i is the fractional bit-width of the i-th tap, Z represents the integer value, and ub indicates the upper bound of the bit-width. Then, the objective function is defined as

$$f(\boldsymbol{bw}) = \sum_{j=1}^{N} bw_j \tag{10}$$

The constraint term is formulated as

$$g(\boldsymbol{bw}) = SNR_{reference} - SNR_{optimize} \tag{11}$$

where $g(\boldsymbol{bw})$ represents the SNR loss under the bit-width configuration $\boldsymbol{bw}$. The $SNR_{reference}$ denotes the reference SNR utilizing the MIMO equalizer with a baseline configuration. In the reference MIMO, all taps are fixed-point quantized to $Q0.15$. The input and output signals are quantized to $Q2.9$. The error signal e is quantized to $Q2.10$. Additionally, the update term $\boldsymbol{delta_{pq}} = \mu \cdot e_p \cdot conj(\boldsymbol{r_q})$is quantized to $Q0.15$. The $SNR_{optimise}$ refers to the SNR after equalization using the optimized equalizer with the bit-width configuration $\boldsymbol{bw}$, and the bit-widths of other variables remain constant. The τ is the set SNR loss threshold. The initial population is defined as

$$I_1 = \{\boldsymbol{bw}_1, \boldsymbol{bw}_2, \ldots, \boldsymbol{bw}_v\} \tag{12}$$

where v denotes the population size.

The bit-width optimization process based on the GA is illustrated in Fig. 4. In each evolutionary cycle, n sets of input signals with different received optical powers (ROPs) are fed into the MIMO equalizer group, as shown in Fig. 4(a). The equalizer group consists of the reference MIMO and the optimized MIMO under evaluation. The tap coefficients of the optimized MIMO are quantized according to the bit-width configuration represented by individuals in the current population, as shown in Fig. 4(b). For each individual in the population, the SNR losses for the n input signal sets are calculated, and the loss vector is

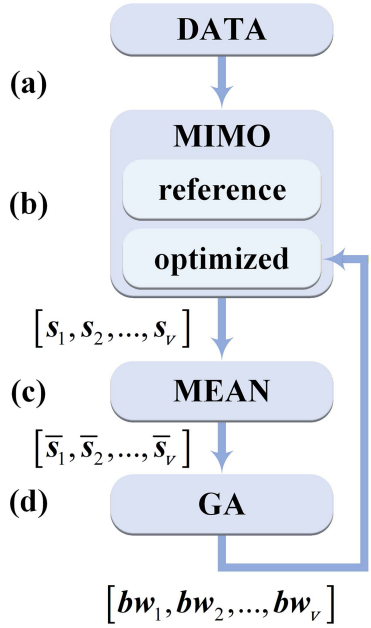

Fig. 4. The GA-based bit-width optimization framework.

expressed as

$$\boldsymbol{s_l} = [g_1(\boldsymbol{bw}_l), \ g_2(\boldsymbol{bw}_l), \ldots, g_j(\boldsymbol{bw}_l)] \ (l = 1, 2, \ldots, v) \tag{13}$$

where $g_j(\boldsymbol{bw}_l)$ represents the SNR loss of the l-th bit-width configuration for the j-th signal.

The SNR losses are then averaged as shown in Fig. 4(c). The process evaluates the performance of each bit-width configuration with different ROPs, enhancing the robustness. The averaged $\overline{s_l}$ serves as the constraint term for the corresponding individual.

The fitness of population individuals is determined by the fitness function. The fitness function incorporates the objective function and introduces a penalty term when the average SNR loss exceeds the constraint τ. The fitness function is defined as

$$fitness(\boldsymbol{bw}) = f(\boldsymbol{bw}) + \alpha \cdot \max(0, \overline{s_l} - \tau) \tag{14}$$

where α denotes the penalty factor, and τ indicates the SNR constraint. The lower $fitness(\boldsymbol{bw})$ indicates fewer total bit-widths.

In Fig. 4(d), the new population individuals are generated by selection, crossover, and mutation operations. The selection operation employs a roulette wheel strategy, where the selection probability is assigned based on fitness values. The high-fitness individuals have a greater retention probability, while the low-fitness individuals are more likely to be eliminated. During the crossover, the genes at identical positions are exchanged between randomly paired parent individuals with a predefined probability. In the end, the mutation is applied by randomly altering the value of a single gene within an individual with a low probability. These genetic operators enhance population diversity through feature recombination and controlled randomization, facilitating global optimization. The evolutionary process terminates when either the maximum generation count is reached or the optimum objective function shows no improvement for L consecutive generations. The historical best bit-width configuration is adopted as the final solution.

B. Elimination of Redundant Bit-Widths

After the GA-based bit-width configuration optimization, the original tap $\boldsymbol{h}$is transformed into $\boldsymbol{h}'$. The numerical relationship between $\boldsymbol{h}$ **and** $\boldsymbol{h}'$ is given by (4). Based on this, the convolution operation of the equalizer is expressed as

$$y(k) = \sum_{n=-N}^{N} h'(n) \cdot r(k-n) \tag{15}$$

Subsequently, amplitude statistics of h' are performed to define the numerical range of each tap throughout the entire adaptation process. This ensures that the designed bit-width allocation prevents overflow. Even in rare cases where overflow occurs, fluctuations in tap coefficients exert a limited impact on the overall convergence performance. The inherent robustness of the adaptive algorithm allows for the correction of minor disturbances. Based on the derived dynamic range, redundant bits per tap are identified and removed. Then, (15) is transformed into

$$y(k) = \sum_{n=-N}^{N} \left(h'(n) \cdot 2^{d_i}\right) \cdot r(k-n) \cdot 2^{-d_i} \tag{16}$$

where d_i denotes the number of redundant bits for the i-th tap. Each product requires d_i sign bits extension for the result correction. After the bit-width optimization and redundant bit removal, the deployment of a simplified adaptive MIMO equalizer is performed on an FPGA to verify the effectiveness of the proposed scheme.

IV. FPGA Implementation of Simplified Adaptive MIMO Equalizers

The high-throughput digital signal processing (DSP) in an FPGA is achieved by parallelization [28]. For dual-polarization M-ary QAM signals, the relationship between signal rate r, clock frequency f, and parallelism p is shown in (17).

$$r = 2 \times \log_2 M \times f \times p \tag{17}$$

When p increases, an FPGA can handle the higher-rate signal. The pipelined implementation of the equalizer is shown in Fig. 5. The signal is buffered by multi-level register banks of length $p+N-1$. The registers in the green dashed box are designed to store p parallel input signals and are updated every clock cycle in Fig. 5(a). The registers in the yellow dashed box are utilized to create an overlap of $N-1$ signal samples. They receive data from the registers in the red dashed box every clock cycle. In Fig. 5(b), A window with the length N slides to allocate the required input for the MIMO equalizer of each channel.

The implementation diagram of the p-channel dual-polarization adaptive time-domain MIMO equalizer is shown in Fig. 5(c). The inputs for X- and Y-polarizations of the j-th channel and k-th clock cycle are represented by $r_x[(k-1)p+j:(k-1)p+j+N-1]$ and $r_y[(k-1)p+j:(k-1)p+\mathrm{j}+N-1]$ The corresponding outputs for X- and Y-polarizations are represented by $z_x((k-1)p+j)$ and $z_y((k-1)p+j)$. To reduce the computational overhead, the tap coefficients are updated in the shared feedback modules, and the remaining channels share the updated result. The n_1, n_2, and n_m correspond, respectively, to the channel indices employed for tap coefficient updating, with m representing their count. The error signals are denoted as e_{x} and e_{y}. The update amount for tap coefficient $\boldsymbol{h}_{pq}$ is expressed as $\boldsymbol{delta\_pq}$ $(p,q\in\{x,y\})$. The update delay n_{ud} is calculated as

$$n_{ud} = p \cdot n_g \tag{18}$$

where n_g represents the total computational delay of a single channel, which consists of feedforward, error calculation, and update delay. The feedforward delay is calculated as $2+clog_2(2N)$where $clog_2(\cdot)$ denotes the ceiling of the logarithmic operation. The error calculation and update delay are 3 and $2+clog_2(\mathrm{m})$, respectively. During the tap coefficients update, the new coefficients take effect after a delay of n_{ud} symbols. The lack of timely update of the tap coefficients reduces the capability of the equalizer to track rapid channel variations.

In the FPGA implementation, the tap coefficient update process is illustrated in Fig. 6. The tap coefficient h is the fixed-point number with the $Q0.d+u$format, and the $delta$ is defined as the update increment of h. Firstly, the u effective bits of h are extracted by the left-shift operation as h'. Secondly, the $delta'$ is obtained through the left-shift operation by d bits and the round operation of high-order $u+1$ bits on $delta$. Finally, the updated coefficient h'' is generated by the fixed-point addition of h' and $delta'$.

During deployment, the dataset is stored as fixed-point numbers in the read-only memory (ROM). The equalizer receives p-channel data from ROM for parallel processing. The output signals are captured by ILA for subsequent DSP operations and the calculation of SNR and BER to confirm the effectiveness of the proposed scheme.

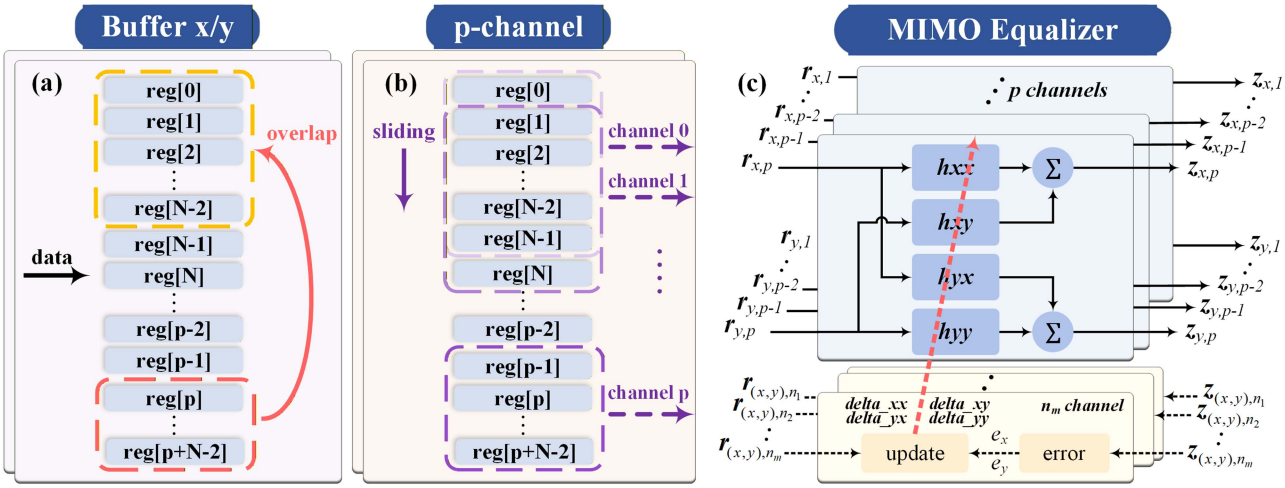

Fig. 5. FPGA implementation of (a) data buffer and (b) data distribution module. (c) Implementation of the p-channel adaptive dual-polarization MIMO equalizer.

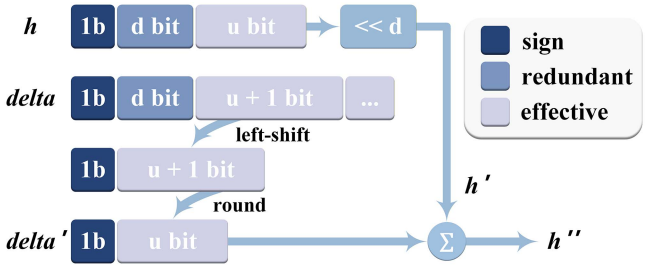

Fig. 6. The process of the tap coefficient update procedure.

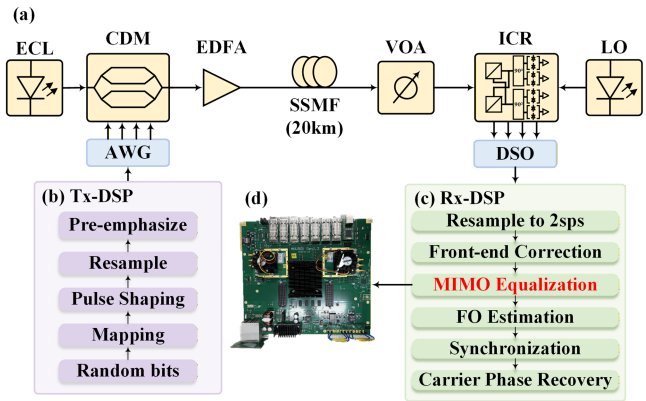

Fig. 7. (a) Experimental setup for a 200G Coherent PON system. (b) Tx-DSP and (c) Rx-DSP procedure. (d) Xilinx VCU118 FPGA development board.

V. Experimental Result

A. Experimental Setup and Offline Performance

The effectiveness of the proposed low-complexity adaptive MIMO equalizer based on hybrid-precision tap bit-width optimization is verified in a polarization-division multiplexed (PDM) coherent PON system transmitting a 200-Gb/s DP-16QAM signal. The corresponding experimental setup is shown in Fig. 7(a). At the transmitter, the random bits are mapped to 16-QAM symbols and shaped using a square root-raised cosine (RRC) filter with a roll-off factor of 0.1 as depicted in Fig. 7(b). After resampling to match the sampling rate of the 4-channel arbitrary waveform generator (AWG) operating at 80GSa/s, the signal is pre-emphasized to compensate for the device bandwidth limitation. Before transmission in a 20-km standard single-mode fiber (SSMF), the electrical signal is modulated by a 40-GHz coherent driver modulator (CDM) and amplified to 8 dBm by an erbium-doped fiber amplifier (EDFA). The external cavity laser (ECL) operating at 1550 nm is the light source with a 14-dBm optical power. At the receiver, the received optical power (ROP) is adjusted by a variable optical attenuator (VOA). The attenuated optical signal is received by a 40-GHz integrated coherent receiver (ICR) and then sampled by two 100-GSa/s Tektronix digital storage oscilloscopes (DSO). Finally, the signal is uploaded to a personal computer (PC) for resampling, front-end correction, channel equalization, frequency offset estimation (FOE), synchronization, and carrier phase recovery (CPR) as shown in Fig. 7(c).

The dataset with 2 samples per symbol is generated after front-end correction and imported into the ROM for real-time equalization in an FPGA. The FPGA is Xilinx VCU118, which is equipped with Virtex UltraScale+ Xcvu9p-flga2104-2l-e as shown in Fig. 7(d). Then, we develop the Verilog hardware description language (HDL) to define the bottom-up underlying circuit and logic framework of the adaptive MIMO equalizer in Vivado. Finally, the equalized signal is captured by an ILA for subsequent DSP.

The offline performance is shown in Fig. 8 to illustrate the BER characteristic. As the memory length of the equalizer increases, the BER decreases. However, the performance improvement is negligible as the memory length increases from 21 to 31. With the launch optical power set to 8dBm, the 21-tap MIMO equalizer yields a 35.13-dB power budget for X-polarization and 35.19-dB for Y-polarization. Further increasing the launch power leads to nonlinear effects, which degrade the BER. Additional nonlinear equalizer is required for compensation. Therefore, 8 dBm is a suitable choice that balances both the

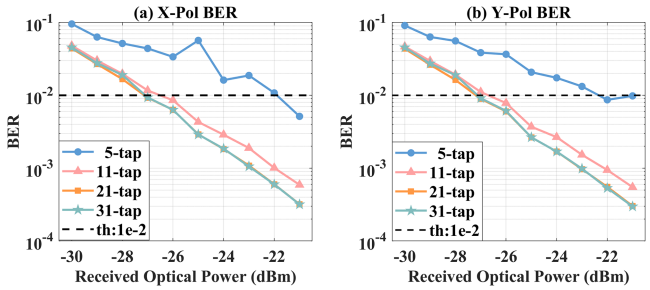

Fig. 8. Offline performance with different ROPs.

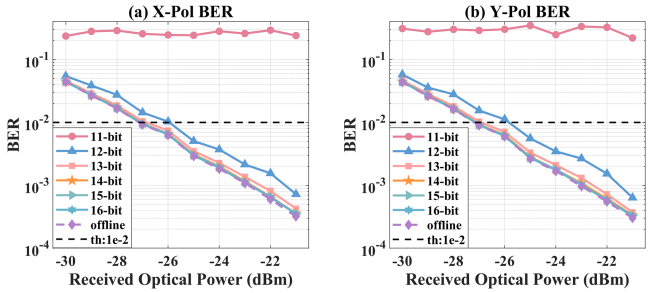

Fig. 9. Real-time single-channel equalization performance with different tap bit-widths.

power budget and system performance. Finally, a 21-tap MIMO equalizer is employed for subsequent bit-width optimization and hardware implementation.

B. FPGA Implementation of the Single-Channel MIMO Equalizer With Uniform Tap Bit-Widths

Fig. 9 demonstrates the performance when applying a 21-tap MIMO equalizer for single-channel real-time equalization in an FPGA. All tap bit-widths are kept consistent. Compared with the offline model, the 16-bit equalizer exhibits a negligible performance penalty. This is attributed to the high-precision quantization and low update latency of the single-channel implementation. Compared to the 16-bit model, a 4-bit reduction in bit-width incurs a 1.24-dB loss in power budget. When the bit-width is 11, the tap coefficients cannot be effectively updated due to the small learning rate, resulting in a sharp performance degradation. The corresponding FPGA resource consumption is illustrated in Fig. 10. The four main resources utilized are LUT, register, CARRY8, and DSP48E2. As the bit-width decreases, the consumption of DSP48E2 slices exhibits no reduction due to the immunity to the variation of bit-width, while the other resources all experience a reduction.

The statistic on the redundant bits of taps is performed when all taps adopt the same quantization bit-width. Fig. 11 illustrates the quantity of redundant bits for taps at different positions in the single-channel 21-tap MIMO equalizer. The central tap exhibits fewer redundant bits due to the larger amplitude. Taps with smaller amplitudes that are farther from the center exhibit more redundant bits, resulting in the waste of hardware resources. The removal of redundant bits can reduce the resource consumption

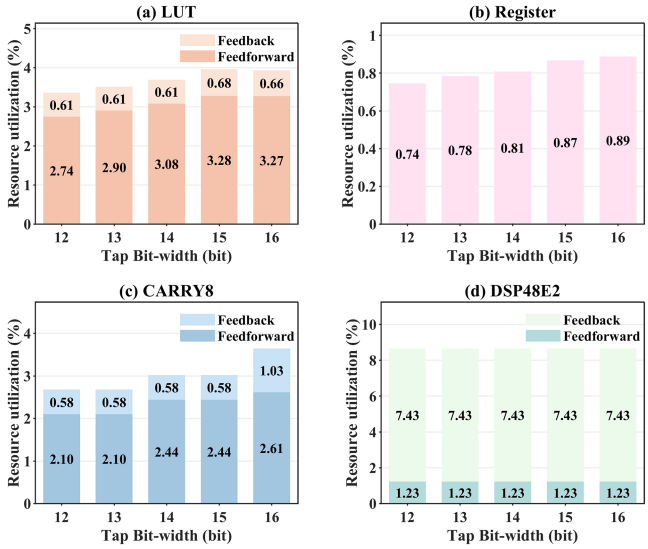

Fig. 10. Resource consumption of FPGA deployment for the single-channel MIMO equalizer with different tap bit-widths.

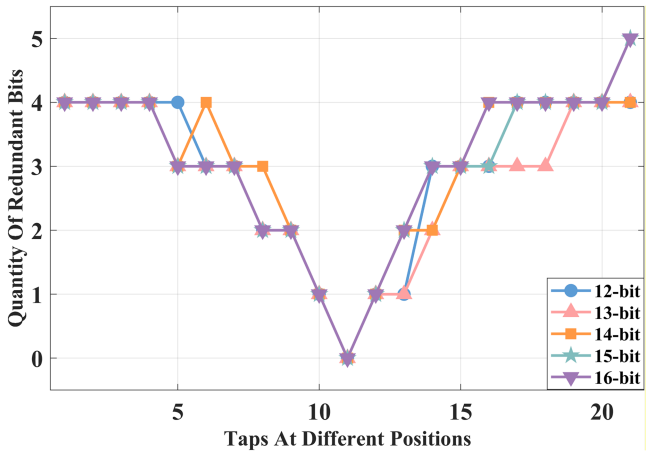

Fig. 11. The quantity of redundant bits for taps at different positions in the single-channel MIMO equalizer with different tap bit-widths.

without sacrificing performance, as illustrated in Fig. 12. The decline is a comparative decrease relative to Fig. 10. The usage of LUT, CARRY8, and register all decreases. Therefore, the removal of redundant, ineffective bits can reduce the overall hardware resource consumption.

C. FPGA Implementation of the Single-Channel MIMO Equalizer Based on Optimized Bit-Widths

The bit-width optimization for a 21-tap MIMO equalizer is implemented in MATLAB. The GA algorithm is employed to search for the optimal bit-width configuration under a specific SNR loss constraint. The population size is set to 50, and the number of iterations is 500. Further increases in the population size and iteration count yield negligible performance improvements while incurring substantial computational overhead. In addition, the crossover ratio is configured as 0.8 to enhance the

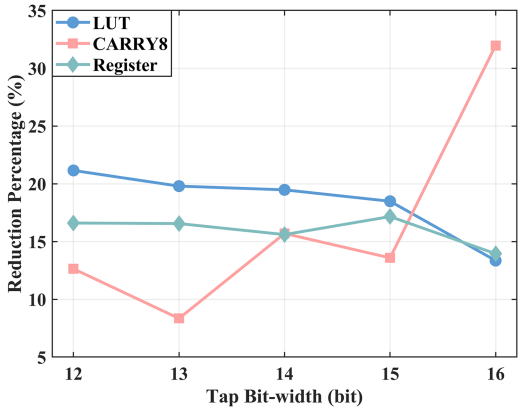

Fig. 12. The percentage reduction in resources after removing redundant bits in the single-channel MIMO equalizer.

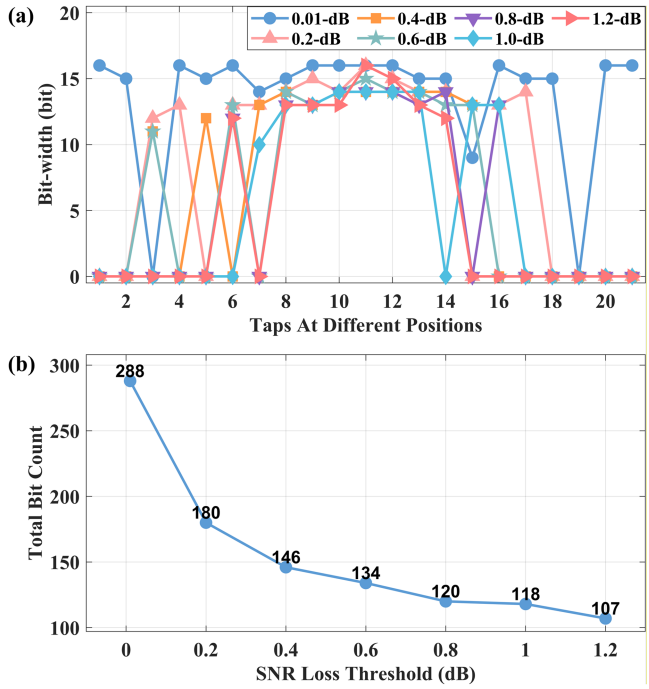

Fig. 13. (a) The optimized bit-width distributions and (b) the total bit count with different SNR loss thresholds.

efficiency of genetic information exchange within the population and accelerate the search for optimal bit-width configurations. The tolerance is set to 1e-6, and the elite count is specified as 5% of the population size to retain optimal bit-width configurations while preserving population diversity. Fig. 13(a) illustrates the optimized bit-width distributions with different SNR loss thresholds. As the SNR loss threshold increases, more tap bit-widths are set to 0, meaning they are clipped, and the total bit-width also decreases gradually as shown in Fig. 13(b). However, when the SNR loss threshold exceeds 0.6 dB, the total bit-width decreases slowly. Compared to the 0.6-dB SNR loss threshold, the total bit-width decreases by only 27 bits at the 1.2-dB threshold.

The optimized equalizer is deployed on FPGA for performance evaluation, as shown in Fig. 14. The corresponding

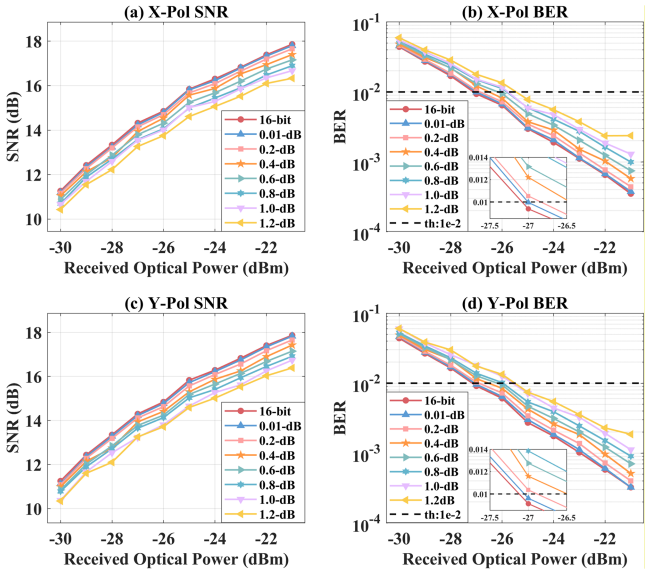

Fig. 14. The performance of single-channel FPGA deployment using the bit-width optimized MIMO equalizer.

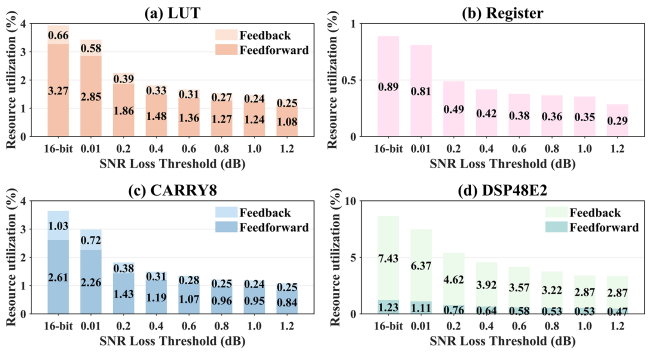

Fig. 15. The resource consumption of single-channel FPGA deployment using the bit-width optimized MIMO equalizer.

FPGA resource consumption of single-channel MIMO equalizer is shown in Fig. 15. Compared to the 16-bit equalizer, the equalizer optimized with the 0.01-dB SNR loss threshold exhibits the power budget losses of only 0.11 dB and 0.08 dB in the X and Y polarizations, respectively. The usage of LUT, register, CARRY8, and DSP48E2 decreases by 12.92%, 8.90%, 18.13%, and 13.51%, respectively. Further increasing the SNR loss threshold can reduce the resource consumption, but also causes performance degradation. When the SNR loss threshold is 0.4 dB, the power budget losses are 0.60 dB and 0.62 dB, respectively. Meanwhile, the usage of LUT, register, CARRY8, and DSP48E2 decreases by 53.99%, 52.98%, 59.06%, and 47.30%, respectively. Increasing the SNR loss threshold to 1.2 dB causes power budget losses of up to 1.65 dB and 1.64 dB in X and Y polarizations. However, the rate of resource consumption reduction decelerates. Therefore, the reasonable range for the SNR loss threshold is less than 0.8 dB. After bit-width optimization, redundant bits are removed without affecting performance, as shown in Fig. 16. The usage of LUT, CARRY8, and register

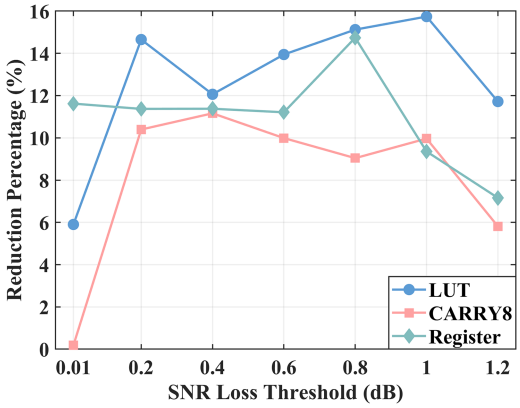

Fig. 16. The percentage reduction in resources after removing redundant bits in the bit-width optimized MIMO equalizer.

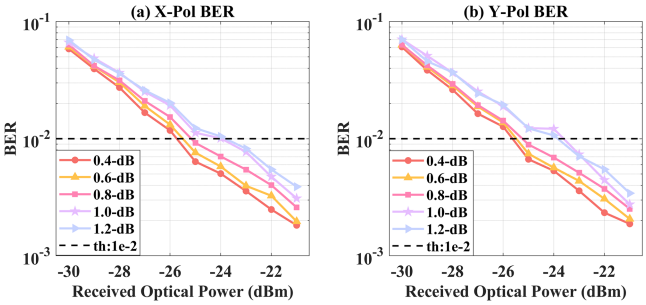

Fig. 17. The performance of the 50-channel MIMO equalizer.

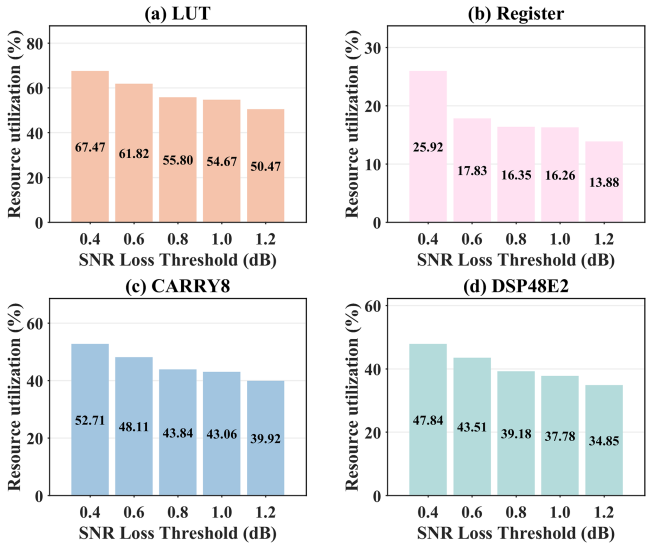

Fig. 18. The resource consumption of the 50-channel MIMO equalizer in an FPGA.

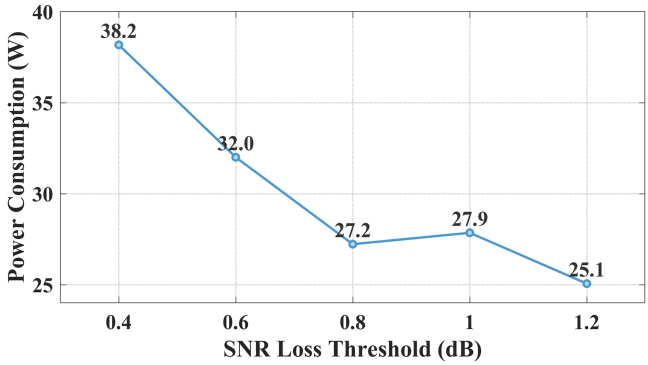

Fig. 19. The power of the 50-channel MIMO equalizer in an FPGA.

all decreases. The decline is a comparative decrease relative to Fig. 15. Compared to Fig. 12, the percentage reduction is diminished owing to the pruning of certain unimportant taps during the optimization process.

D. Multi-Channel FPGA Implementation of MIMO Equalizer After Bit-Width Optimization

After bit-width optimization and redundant bit removal, the simplified MIMO equalizer is deployed on an FPGA in the multi-channel mode. Due to resource and timing constraints, the parallelism is 50, the clock frequency is 250 MHz, and the corresponding throughput is 100 Gb/s. It is crucial to emphasize that the parallelism is at the symbol level and the step size of the sliding window is 2 samples in Fig. 5 when the input signal is sampled at two points per symbol. The FPGA has a lower clock frequency due to routing resource constraints, while the ASIC chip has a higher clock frequency, up to over 500 MHz [29]. The higher clock frequency enables a higher real-time rate and can reduce the degree of parallelism to lower the resource consumption. Fig. 17 shows the performance of the 50-channel MIMO equalizer in the FPGA. Compared to the performance of the single-channel MIMO equalizer shown in Fig. 14, the performance of the 50-channel one degrades due to the feedback latency caused by the high parallelism. When the SNR loss threshold is 0.4 dB, the power budgets of X and Y polarizations are 33.73 dB and 33.63 dB, respectively. Compared to the single-channel implementation, the power budget losses of X and Y polarizations caused by the feedback latency are 0.78 dB and 0.90 dB, respectively. This is because the feedback latency hampers the timely update of the tap coefficients, while high parallelism contributes to a reduction in update frequency. Both factors degrade the ability of the equalizer to track rapid channel variations. In addition, the higher SNR loss threshold leads to further degradation in performance. For the SNR loss threshold of 1.2 dB, the power budgets of X and Y polarizations are 31.81 dB and 31.84 dB, respectively. This represents the decrease of 1.92 dB and 1.89 dB, as opposed to the 0.4-dB SNR loss threshold. The FPGA resource consumption of the 50-channel MIMO equalizer is shown in Fig. 18. The most utilized resources are LUT, CARRY8, and DSP48E2, which are used to implement arithmetic operations. For the 0.4-dB SNR loss threshold, LUT, CARRY8, and DSP48E2 account for 67.47%, 52.71%, and 47.84% of the total resources, respectively. In contrast, the register accounts for only 25.92%. When the SNR loss threshold increases, the resource consumption decreases gradually. Compared to the 0.4-dB threshold, the LUT, Register, CARRY8, and

DSP48E2 at the 1.2-dB threshold show an additional decrease of 17.00%, 12.04%, 12.79%, and 12.99% of the total resources, respectively. There are still idle FPGA resources available to increase the real-time rate. Fig. 19 illustrates the corresponding power consumption which is measured using the Xilinx Vivado Power Analysis tool based on post-implementation design files. The power consumption of 38.2 W is achieved at the threshold of 0.4 dB. Further increasing the threshold also results in a further reduction in power consumption, thereby validating the effectiveness of our proposed method.

VI. Conclusion

To reduce the complexity of the adaptive MIMO equalizer, we propose a hybrid-precision tap bit-width optimization method. By reducing the effective bit-width and removing redundant bits, the hardware overhead of the equalizer is significantly reduced with slight performance loss. The strategy is orthogonal to the simplified structural designs and can be applied to various equalizer architectures. When the SNR loss threshold is 0.4 dB, the LUT, Register, CARRY8, and DSP48E2 are reduced by 59.54%, 58.33%, 63.63% and 47.30% after removing redundant bits, respectively, thus demonstrating the effectiveness of the proposed method. Finally, the simplified equalizer is deployed in parallel to achieve a real-time rate of 100 Gb/s. The power budgets for X and Y polarizations are 33.73 dB and 33.63 dB, respectively, and the power consumption is 38.2 W. In summary, our proposed method applies to equalizers of any structure and is expected to be applied in 200G PON to reduce the chip power consumption.

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